Application Number: 10/604,573 Examiner: Shawn Riley Art Unit: 2838

February 3, 2005

Resubmission of Office Action Reply due to Non-Compliance 37 C.F.R. 1.121

Signature

The following 15 sheets are a retransmition by facsimile identical to the Office Action Reply submitted on January 10, 2005 to the United States Patent and Trademark Office for application number 10/604,573 entitled System and Method for Integrating a Digital Core with a Switch Mode Power Supply, with the addition of the Signature Page submitted separately on February 1, 2005. Today's retransmission complies with the instructions given by telephone by Legal Instruments Examiner Tracey Young, Telephone Number (571) 272-1644, on Wednesday, February 2, 2005, recommending retransmission in its entirety despite today's retransmission creating duplicates of the documents originally transmitted on January 10, 2005 and February 1, 2005. Today's retransmission shall be deemed authentic by virtue of the signature hereunder of Andrew R. Gizara, the sole inventor and applicant.

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Andrew R. Gyara February 3, 2005 PEST ANABLE COPY

Facsimile Transmission Cover Page, 16 pages total including this page

January 10, 2005

UNITED STATES PATENT OFFICE ACTION REPLY

FOR

(TITLE):

SYSTEM AND METHOD FOR INTEGRATING A DIGITAL CORE WITH A SWITCH MODE POWER **SUPPLY**

APPLICANT:

ANDREW R. GIZARA

APPLICATION NUMBER:

10/604,573

FILING DATE:

07/31/2003

EXAMINER:

SHAWN RILEY

ART UNIT:

2838

PREPARED BY:

Andrew R. Gizara 24471 Corta Cresta Drive Lake Forest, California 92630-3914 (949) 457-0751

Office Action Reply Page 1 of 14

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Application Number: 10/604,573

Examiner: Shawn Riley Art Unit: 2838

January 10, 2005

Specification

REPLY TO DETAILED ACTION

The final page of this Office Action Reply includes the currently amended Abstract of the disclosure to replace in its entirety the original Abstract. The currently amended abstract is a subset of the original Abstract, length reduced to less than 150 words and having removed legal phraseology, i.e. "said", a subset with the exception of adding the adjectives "digital open-loop" before the term "output voltage fixing circuitry" in order to include that which is new in the art to which the invention pertains.

Claim Objections

Subsequent pages of this Office Action Reply include the currently amended Claims. Claim 15 has been revised to depend solely on claim 9, with the applicable clause from claim 14, "a substrate of fiberglass resin epoxy of type FR4 based laminate material" explicitly stated in the claim text of claim 15.

All claims have been revised for proper use of punctuation, particularly use of colons, semicolons and commas. For instance, all dependent claims at a minimum have

been revised to include a missing comma immediately following the referenced claim

number. Many of the revised claims now use improved legal phraseology with terms

"said", "comprising", "further comprising", and "wherein". Indentation shown in the

currently amended claims is preferred compared to the original claims because undesired

differences may be apparent due to the applicant's inability to observe and edit the final

Office Action Reply Page 2 of 2 14

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Application Number: 10/604,573 Examiner: Shawn Riley Art Unit: 2838 January 10, 2005 electronically packaged version of the application submitted through the Electronic Filing System.

Claim Rejections

Claims 2 and 3 have been canceled because the applicant cannot point out patentable novelty in claims 2 and 3 in their broad form in view of the state of the art disclosed by the cited references.

However, the applicant hereby requests reconsideration of claim 1 as amended to include within the clause of "output voltage fixing circuit", the further limitation of "digital open-loop output voltage fixing circuit". The applicant asserts this does not introduce new matter under 37 C.F.R. 1.121(f) as the original specification presents digital open-loop terminology in no less than two instances. The last sentence in the Summary of Invention introduces the open-loop configuration: "... the present invention's substantial departure from prior art and significant novelty exists in the preferred embodiment wherein said switch mode synchronous DC-to-DC step-down converter is implemented in an open-loop configuration retaining precision based on semiconductor die power consumption characterization data...". Most precisely the original specification states this novelty of digital open-loop configuration in the last sentence of paragraph 32 in the Detailed Description describing Figure 6, "The equation in block 601 and its derivation verifies the assertion of the fundamental theoretical principle of the present invention, namely, given fixed input and output voltages 101, 102, and having

Office Action Reply Page 3 of # 14

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Art Unit: 2838 January 10, 2005 Application Number: 10/604,573 Examiner: Shawn Riley characterization data defining all supply current states Io, with empirical data or even reasonably accurate estimates stating the component losses, one may digitally fix the duty cycle of a high efficiency synchronous switch mode power supply in an open loop configuration and still obtain a precise output voltage 102 while eliminating the expense of the frequency compensated feedback loop and especially the precision analog circuits internal to the semiconductor die 100". This very sentence also clearly points out the patentable novelty over the cited reference Rozsypal (U.S. Patent 6,781,353) as well as the cited reference Ito et al. (U.S. Patent 6,683,767). Rosypal (U.S. Patent 6,781,353) clearly states, "Error amplifier 247 is a standard analog amplifier formed in the regulation feedback path..." in line 9 of column 5, implying an analog closed-loop voltage control algorithm. Also in the invention of Rozsypal (U.S. Patent 6,781,353), comparators 220, 230, 247 and current references 242, 246 are analog components that fix the output voltage in a closed-loop configuration, the closed-loop being defined by the path from the output voltage back through the analog comparators 220, 230, 247 through the logic blocks 221, 250 which directly control the output voltage. Likewise, Ito et al. (U.S. Patent 6,683,767) presents a plurality of analog precision components internal to the semiconductor, i.e. the reference voltage generators 60, 100, and particularly the differential amplifier 41 and reference voltage buffer 110. While Ito et al. (U.S. Patent 6,683,767) does not detail the control algorithm for precise output voltage control of the switch mode power supply, an analog reference voltage generator 110 is clearly depicted in Figures 29 and 30 for such use. Thus while the references cited preclude the present

Office Action Reply Page 4 of 4/4

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January 10, 2005 Application Number: 10/604,573 Examiner: Shawn Riley Art Unit: 2838 invention's claim 1 in its original broad form, the currently amended claim 1 with the further limitation of "digital open-loop output voltage fixing circuit" best describes in broadest form the patentable novelty over the references cited.

The applicant hereby requests reconsideration of claim 14 in its currently amended form. Once again, the further limitation of the clause: "digital open-loop output voltage fixing circuit" renders this currently amended claim 14 patentable over the references cited based on the same argument for reconsidering the currently amended claim 1.

Allowable Subject Matter

Claims 4-6 and 9-13 per the recommendation of the examiner have been rewritten such that claim 4 now exists in independent form including all of the limitations of the original base claim 1 and the further limiting clause of the original claim 4. The remaining claims addressed by this comment in the first Office Action, Claims 5, 6, and 9-13 now being dependent upon claim 4 in their currently amended form all presently fall into the category of allowable subject matter as stated in the first Office Action.

The applicant hereby requests reconsideration of claims 7 and 8 because in their currently amended form these claims now have dependence upon claim 4 instead of dependence upon claim 1 as in their original form and therefore with the currently

Office Action Reply Page 5 of 8 14

Application Number: 10/604,573 Examiner: Shawn Riley Art Unit: 2838 January 10, 2005 amended claim 4, the scope of claims 7 and 8 have also narrowed to include the subject matter of patentable novelty of claim 4.

Conclusion

Claim 4, per the recommendation of the examiner, having been rewritten such that claim 4 now exists in independent form, increases the total number of independent claims in the application by one. Therefore, the applicant concurrent to this facsimile transmittal has paid the fee defined in 37 C.F.R 1.16(b) for a small entity defined by 37 C.F.R. 1.27(a) for the additional independent claim. Since the examiner has indicated allowable subject matter, the applicant may subsequently request an international-type search report under 37 C.F.R. 1.104(a)(4). The applicant can be reached at (949) 457-0751 from 9am-10:30 am EDT Monday through Friday, or else a voice mail or facsimile message may be left at that telephone number at any time. The applicant's email address is: gizara@cox.net and is a preferred means of communication.

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Application Number: 10/604,573 Examiner: Shawn Riley Art Unit: 2838

January 10, 2005

SIGNATURE PAGE UNDER 37 C.F.R. 1.4

Signature

This certifies that the Office Action Reply submitted on January 10, 2005 with the United States Patent and Trademark Office for application number 10/604,573 entitled

System and Method for Integrating a Digital Core with a Switch Mode Power Supply shall be deemed authentic by virtue of the signature hereunder of Andrew R. Gizara, the sole inventor and applicant.

Andrew R. Gizera, January 10, 2005

Office Action Reply Last Page

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